AMENDMENTS TO THE CLAIMS

This listing of the claims, if entered, will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (Currently Amended) A method of signal delay adjustment comprising:

receiving a first input signal having a first phase and a second input signal having a second phase;

receiving a first control signal, a second control signal, and a third control signal;

generating a first signal having a third phase between said first phase and said second phase, said third phase determined by said first control signal;

generating a second signal having a fourth phase between said first phase and said second phase, said fourth phase determined by said second control signal; and

generating a third signal having a fifth phase between said third phase and said fourth phase, said fifth phase determined by said ~~fourth~~ third control signal.

2. (Original) The method of claim 1 wherein said first phase and said second phase have a predetermined phase difference.

3. (Original) The method of claim 1 wherein said first control signal comprises data indicative of a first weighting factor of said first input signal and a second weighting factor of said second input signal.

4. (Original) The method of claim 1 wherein said second control signal comprises data indicative of a first weighting factor of said first input signal and a second weighting factor of said second input signal.

5. (Original) The method of claim 1 wherein said third control signal comprises data indicative of a first weighting factor of said first signal and a second weighting factor of said second signal.

6. (Original) The method of claim 1 further comprising:

receiving a reference signal;

delaying said reference signal to generate said first input signal having said first phase; and

delaying said reference signal to generate said second input signal having said second phase, wherein said first phase and said second phase have a predetermined phase difference.

7. (Original) The method of claim 6 further comprising:

comparing said reference signal with said third signal;

determining whether said fifth phase of said third signal should be increased or decreased; and

setting said control signals in response to said determining.

8. (Original) A method of signal delay adjustment comprising:

receiving a first input signal having a first

phase and a second input signal having a second phase;

receiving a first control signal, a second control signal, a third control signal, a fourth control signal, and a fifth control signal;

generating a first signal having a third phase between said first phase and said second phase, said third phase determined by said first control signal;

generating a second signal having a fourth phase between said first phase and said second phase, said fourth phase determined by said second control signal;

generating a third signal having a fifth phase between said third phase and said fourth phase, said fifth phase determined by said third control signal;

generating a fourth signal having a sixth phase between said third phase and said fourth phase, said sixth phase determined by said fourth control signal; and

generating a fifth signal having a seventh phase between said fifth phase and said sixth phase, said seventh phase determined by said fifth control signal.

9. (Original) A method of signal delay adjustment comprising:

receiving a reference signal;

delaying said reference signal to generate a first signal having a first phase;

delaying said reference signal to generate a second signal having a second phase;

generating a third signal having a third phase between said first phase and said second phase;

generating a fourth signal having a fourth phase between said first phase and said second phase, said fourth phase not equal to said third phase; and

generating a fifth signal having a fifth phase between said third phase and said fourth phase.

10. (Origina l) The method of claim 9 further comprising:

comparing said reference signal with said fifth signal;

determining whether said fifth phase of said fifth signal should be increased or decreased; and

adjusting said fifth phase in response to said determining.

11. (Original) The method of claim 9 further comprising:

receiving a first control signal before said delaying said reference signal to generate said first signal;

receiving a second control signal before said delaying said reference signal to generate said second signal;

receiving a third control signal before said generating said third signal;

receiving a fourth control signal before said generating said fourth signal; and

receiving a fifth control signal before said generating said fifth signal.

12. (Original) The method of claim 11 wherein:

said first control signal comprises data indicative of said first phase by which said reference signal is to be phase-shifted to generate said first signal; and

said second control signal comprises data indicative of said second phase by which said reference signal is to be phase-shifted to generate said second signal, wherein

said first phase and said second phase have a predetermined phase difference.

13. (Original) The method of claim 11 wherein said third control signal comprises data indicative of a first weighting factor of said first signal and a second weighting factor of said second signal.

14. (Original) The method of claim 11 wherein said fourth control signal comprises data indicative of a first weighting factor of said first signal and a second weighting factor of said second signal.

15. (Original) The method of claim 11 wherein said fifth control signal comprises data indicative of a first weighting factor of said third signal and a second weighting factor of said fourth signal.

16. (Previously Presented) A method of signal delay adjustment comprising:

a) generating a first output signal having a first phase between the phases of first and second input signals;

b) generating a second output signal having a second phase not equal to said first phase between the phases of said first and second input signals;

c) repeating a) and b) a predetermined number of times greater than one, wherein:

said first output signal generated from a preceding step a) is said first input signal in subsequent steps a) and b), and

said second output signal generated

from a preceding step b) is said second input signal in said subsequent steps a) and b); and

d) generating a third output signal having a third phase between said first phase of said first output signal and said second phase of said second output signal generated from step c) after said predetermined number of times.

17. (Original) Circuit apparatus comprising:

a first digital phase mixer having a first input operative to receive a first input signal having a first phase, a second input operative to receive a second input signal having a second phase, a third input operative to receive a first control signal, and an output, said first digital phase mixer generating a first output signal having a third phase between said first phase and said second phase based on said first control signal;

a second digital phase mixer having a first input operative to receive said first input signal, a second input operative to receive said second input signal, a third input operative to receive a second control signal, and an output, said second digital phase mixer generating a second output signal having a fourth phase between said first phase and said second phase based on said second control signal; and

a third digital phase mixer having a first input operative to receive said first output signal, a second input operative to receive said second output signal, a third input operative to receive a third control signal, and an output, said third digital phase mixer generating a third output signal having a fifth phase between said third phase and said fourth phase based on said third control signal.

18. (Original) Th e apparatus of claim 17 wherein said first control signal comprises data indicative of a first weighting factor of said first input signal and a second weighting factor of said second input signal.

19. (Original) The apparatus of claim 17 wherein said second control signal comprises data indicative of a first weighting factor of said first input signal and a second weighting factor of said second input signal.

20. (Original) The apparatus of claim 17 wherein said third control signal comprises data indicative of a first weighting factor of said first output signal and a second weighting factor of said second output signal.

21. (Original) The apparatus of claim 17 further comprising a variable digital delay line operative to receive a reference signal and a fourth control signal, and to output said first input signal and said second input signal, wherein said first input signal and said second input signal are phase-shifted signals of said reference signal based on said fourth control signal and have a predetermined phase difference.

22. (Original) The apparatus of claim 21 further comprising a phase detector operative to receive said reference signal and said third output signal, and to output a signal at said output indicative of whether said fifth phase should be increased or decreased.

23. (Original) The apparatus of claim 22 further comprising control logic operative to receive said signal from said phase detector and to output said control signals.

24. (Original) The apparatus of claim 17 further comprising:

a first variable digital delay line operative to receive a reference signal and a fourth control signal, and to output said first input signal based on said fourth control signal; and

a second variable digital delay line operative to receive said reference signal and a fifth control signal, and to output said second input signal based on said fifth control signal, wherein said first input signal and said second input signal are phase-shifted signals of said reference signal and have a predetermined phase difference.

25. (Original) The apparatus of claim 24 further comprising a phase detector operative to receive said reference signal and said third output signal, and to output a signal indicative of whether said fifth phase should be increased or decreased.

26. (Original) The apparatus of claim 25 further comprising control logic operative to receive said signal from said phase detector, and to output said control signals.

27. (Original) Circuit apparatus comprising:

a first digital phase mixer having a first input operative to receive a first input signal having a first phase, a second input operative to receive a second input signal having a second phase, and an output, said first

digital phase mixer generating a first output signal having a third phase between said first phase and said second phase;

a second digital phase mixer having a first input operative to receive said first input signal, a second input operative to receive said second input signal, and an output, said second digital phase mixer generating a second output signal having a fourth phase between said first phase and said second phase;

a third digital phase mixer having a first input operative to receive said first output signal, a second input operative to receive said second output signal, and an output, said third digital phase mixer generating a third output signal having a fifth phase between said third phase and said fourth phase;

a fourth digital phase mixer having a first input operative to receive said first output signal, a second input operative to receive said second output signal, and an output, said fourth digital phase mixer generating a fourth output signal having a sixth phase between said third phase and said fourth phase; and

a fifth digital phase mixer having a first input operative to receive said third output signal, a second input operative to receive said fourth output signal, and an output, said fifth digital phase mixer generating a fifth output signal having a seventh phase between said fifth phase and said sixth phase.

28. (Original) A digital delay -locked loop circuit comprising:

a first variable digital delay line operative to receive a reference signal and a first control signal, and to output a first output signal having a first phase based on

said first control signal;

a second variable digital delay line operative to receive said reference signal and a second control signal, and to output a second output signal having a second phase based on said second control signal;

a first digital phase mixer operative to receive said first output signal, said second output signal, and a third control signal, and to output a third output signal having a third phase between said first phase and said second phase based on said third control signal;

a second digital phase mixer operative to receive said first output signal, said second output signal, and a fourth control signal, and to output a fourth output signal having a fourth phase between said first phase and said second phase based on said fourth control signal; and

a third digital phase mixer operative to receive said third output signal, said fourth output signal, and a fifth control signal, and to output a fifth output signal having a fifth phase between said third phase and said fourth phase based on said fourth control signal.

29. (Original) The circuit of claim 28 further comprising a phase detector operative to receive said reference signal and said fifth output signal, and to output a signal indicative of whether said fifth phase should be increased or decreased.

30. (Original) The circuit of claim 29 further comprising control logic operative to receive said signal from said phase detector, and to output said control signals.

31. (Original) The circuit of claim 28 wherein:

said first control signal comprises data indicative of said first phase by which said reference signal is to be phase-shifted to generate said first output signal; and

said second control signal comprises data indicative of said phase by which said reference signal is to be phase-shifted to generate said second output signal, where said first phase and said second phase have a predetermined phase difference.

32. (Original) The circuit of claim 28 wherein said third control signal comprises data indicative of a first weighting factor of said first output signal and a second weighting factor of said second output signal.

33. (Original) The circuit of claim 28 wherein said fourth control signal comprises data indicative of a first weighting factor of said first output signal and a second weighting factor of said second output signal.

34. (Original) The apparatus of claim 28 wherein said fifth control signal comprises data indicative of a first weighting factor of said third output signal and a second weighting factor of said fourth output signal.

35. (Currently Amended) Apparatus for signal delay adjustment comprising:

means for receiving a first input signal having a first phase and a second input signal having a second phase;

means for receiving a first control signal, a second control signal, and a third control signal;

means for generating a first signal having a third phase between said first phase and said second phase, said third phase determined by said first control signal;

means for generating a second signal having a fourth phase between said first phase and said second phase, said fourth phase determined by said second control signal; and

means for generating a third signal having a fifth phase between said third phase and said fourth phase, said fifth phase determined by said ~~fourth~~ third control signal.

36. (Currently Amended) Apparatus for ~~of~~ signal delay adjustment comprising:

means for receiving a reference signal;

means for delaying said reference signal to generate a first signal having a first phase;

means for delaying said reference signal to generate a second signal having a second phase;

means for generating a third signal having a third phase between said first phase and said second phase;

means for generating a fourth signal having a fourth phase between said first phase and said second phase, said fourth phase not equal to said third phase; and

means for generating a fifth signal having a fifth phase between said third phase and said fourth phase.

37. (Previously Presented) Apparatus for signal delay adjustment comprising:

a) means for generating a first output signal having a first phase between the phases of first and second input signals;

b) means for generating a second output signal having a second phase not equal to said first phase between the phases of said first and second input signals;

c) means for repeating a) and b) a predetermined number of times greater than one, wherein:

said first output signal generated from a preceding step a) is said first input signal in subsequent steps a) and b), and

said second output signal generated from a preceding step b) is said second input signal in said subsequent steps a) and b); and

d) means for generating a third output signal having a third phase between said first phase of said first output signal and said second phase of said second output signal generated from step c) after said predetermined number of times.